W255

200 MHz 24-Output Buffer for 4 DDR or 3 SDRAM DIMMS

Features

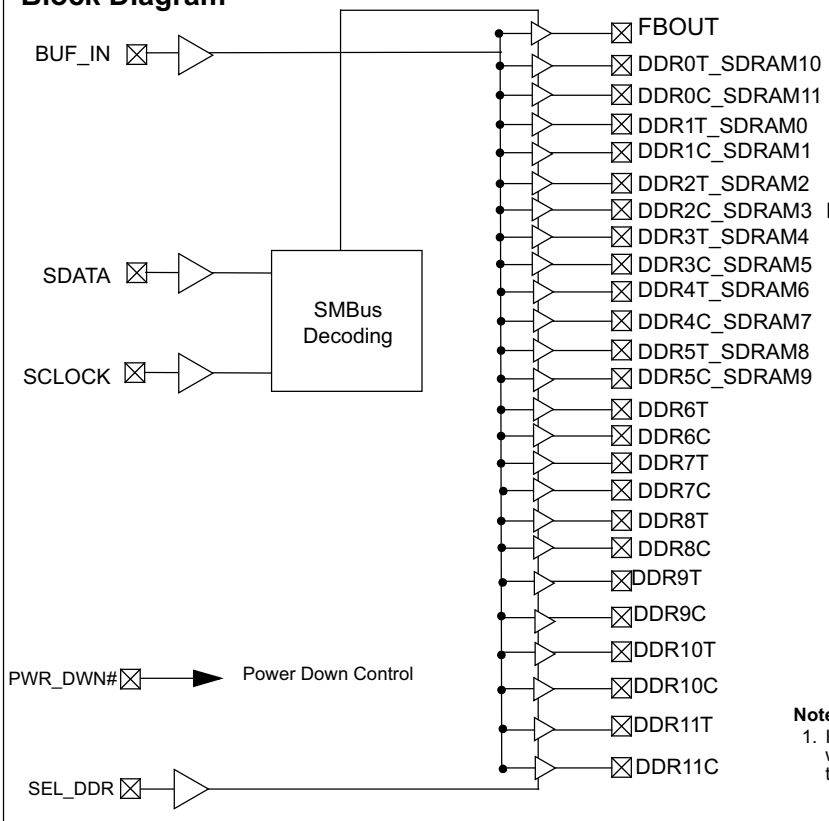
- **One input to 24 output buffer/driver**
- **Supports up to 4 DDR DIMMs or 3 SDRAM DIMMS**
- **One additional output for feedback**
- **SMBus interface for individual output control**
- **Low skew outputs (< 100 ps)**
- **Supports 266-, 333-, and 400 MHz DDR SDRAM**
- **Dedicated pin for power management support**
- **Space-saving 48-pin SSOP package**

Functional Description

The W255 is a 3.3V/2.5V buffer designed to distribute high-speed clocks in PC applications. The part has 24 outputs. Designers can configure these outputs to support four unbuffered DDR DIMMS or to support three unbuffered standard SDRAM DIMMs and two DDR DIMMS. The W255 can be used in conjunction with the W250 or similar clock synthesizer for the VIA Pro 266 chipset.

The W255 also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled (internal pull up).

Block Diagram



Pin Configuration[1]

SSOP
Top View

FBOUT	1	48	SEL_DDR*
VDD3.3_2.5	2	47	VDD2.5
GND	3	46	GND
DDR0T_SDRAM10	4	45	DDR11T
DDR0C_SDRAM11	5	44	DDR11C
DRR1T_SDRAM0	6	43	DDR10T
DDR1C_SDRAM1	7	42	DDR10C
VDD3.3_2.5	8	41	VDD2.5
GND	9	40	GND
DDR2T_SDRAM2	10	39	DDR9T
DDR2C_SDRAM3	11	38	DDR9C
VDD3.3_2.5	12	37	VDD2.5
BUF_IN	13	36	PWR_DWN#*
GND	14	35	GND
DDR3T_SDRAM4	15	34	DDR8T
DDR3C_SDRAM5	16	33	DDR8C
VDD3.3_2.5	17	32	VDD2.5
GND	18	31	GND
DDR4T_SDRAM6	19	30	DDR7T
DDR4C_SDRAM7	20	29	DDR7C
DDR5T_SDRAM8	21	28	DDR6T
DDR5C_SDRAM9	22	27	DDR6C
VDD3.3_2.5	23	26	GND
SDATA	24	25	SCLK

Note:
1. Internal 100K pull-up resistors present on inputs marked with *. Design should not rely solely on internal pull-up resistor to set I/O pins HIGH.

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Pin Summary

Pin Name	Pins	Pin Description
SEL_DDR	48	**Input to configure for DDR-ONLY mode or STANDARD SDRAM mode**. 1 = DDR-ONLY mode. 0 = STANDARD SDRAM mode. When SEL_DDR is pulled HIGH or configured for DDR-ONLY mode, pin 4, 5, 6, 7, 10, 11,15, 16, 19, 20, 21, 22, 27, 28, 29, 30, 33, 34, 38, 39, 42, 43, 44 and 45 will be configured as DDR outputs. Connect VDD3.3_2.5 to a 2.5V power supply in DDR-ONLY mode. When SEL_DDR is pulled LOW or configured for STANDARD SDRAM output, pin 4, 5, 6, 7, 10, 11, 15, 16, 19 and 20, 21, 22 will be configured as STANDARD SDRAM outputs.Pin 27, 28, 29, 30, 33, 34, 38, 39, 42, 43, 44 and 45 will be configured as DDR outputs. Connect VDD3.3_2.5 to a 3.3V power supply in STANDARD SDRAM mode.
SCLK	25	**SMBus clock input**
SDATA	24	**SMBus data input**
BUF_IN	13	**Reference input from chipset**. 2.5V input for DDR-ONLY mode; 3.3V input for STANDARD SDRAM mode.
FBOUT	1	**Feedback clock for chipset**. Output voltage depends on VDD3.3_2.5V.
PWR_DWN#	36	**Active LOW input to enable power-down mode**; all outputs will be pulled LOW.
DDR[6:11]T	28, 30, 34, 39, 43, 45	**Clock outputs**. These outputs provide copies of BUF_IN.
DDR[6:11]C	27, 29, 33, 38, 42, 44	**Clock outputs**. These outputs provide complementary copies of BUF_IN.
DDR[0:5]T_SDRAM [10,0,2,4,6,8]	4, 6, 10, 15, 19, 21	**Clock outputs**. These outputs provide copies of BUF_IN. Voltage swing depends on VDD3.3_2.5 power supply.
DDR[0:5]C_SDRAM [11,1,3,5,7,9]	5, 7, 11, 16, 20, 22	**Clock outputs**. These outputs provide complementary copies of BUF_IN when SEL_DDR is active. These outputs provide copies of BUF_IN when SEL_DDR is inactive. Voltage swing depends on VDD3.3_2.5 power supply.
VDD3.3_2.5	2, 8, 12, 17, 23	**Connect to 2.5V power supply** when W255 is configured for DDR-ONLY mode. Connect to 3.3V power supply, when W255 is configured for standard SDRAM mode.
VDD2.5	32, 37, 41, 47	**2.5V voltage supply**
GND	3, 9, 14, 18, 26, 31, 35, 40, 46	**Ground**

Serial Configuration Map

- The serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  .
  .
  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to “0.”
- SMBus Address for the W255 is:

Table 1.

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

Byte 6: Outputs Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description	Default
Bit 7	–	Reserved, drive to 0	0
Bit 6	–	Reserved, drive to 0	0
Bit 5	–	Reserved, drive to 0	0
Bit 4	1	FBOUT	1
Bit 3	45,44	DDR11T, DDR11C	1
Bit 2	43, 42	DDR10T, DDR10C	1
Bit 1	39, 38	DDR9T, DDR9C	1
Bit 0	34, 33	DDR8T, DDR8C	1

Byte 7: Outputs Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description	Default
Bit 7	30, 29	DDR7T, DDR7C	1
Bit 6	28, 27	DDR6T, DDR6C	1
Bit 5	21, 22	DDR5T_SDRAM8, DDR5C_SDRAM9	1
Bit 4	19, 20	DDR4T_SDRAM6, DDR4C_SDRAM7	1
Bit 3	15,16	DDR3T_SDRAM4, DDR3C_SDRAM5	1
Bit 2	10, 11	DDR2T_SDRAM2, DDR2C_SDRAM3	1
Bit 1	6, 7	DDR1T_SDRAM0, DDR1C_SDRAM1	1
Bit 0	4, 5	DDR0T_SDRAM10, DDR0C_SDRAM11	1

Maximum Ratings

Supply Voltage to Ground Potential.....–0.5 to +7.0V

DC Input Voltage (except BUF_IN)..... –0.5V to V_{DD}+0.5

Storage Temperature.....–65°C to +150°C

Static Discharge Voltage ..... > 2000V (per MIL-STD-883, Method 3015)

Operating Conditions[2]

Parameter	Description	Min.	Typ.	Max.	Unit
VDD3.3	Supply Voltage	3.135		3.465	V
VDD2.5	Supply Voltage	2.375		2.625	V
T_A	Operating Temperature (Ambient Temperature)	0		70	°C
C_{OUT}	Output Capacitance		6		pF
C_{IN}	Input Capacitance		5		pF

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input LOW Voltage	For all pins except SMBus			0.8	V
V_{IH}	Input HIGH Voltage		2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0V			50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}			50	µA
I_{OH}	Output HIGH Current	V_{DD} = 2.375V V_{OUT} = 1V	–18	–32		mA
I_{OL}	Output LOW Current	V_{DD} = 2.375V V_{OUT} = 1.2V	26	35		mA
V_{OL}	Output LOW Voltage[3]	I_{OL} = 12 mA, V_{DD} = 2.375V			0.6	V
V_{OH}	Output HIGH Voltage[3]	I_{OH} = –12 mA, V_{DD} = 2.375V	1.7			V
I_{DD}	Supply Current[3] (DDR-only mode)	Unloaded outputs, 133 MHz			400	mA
I_{DD}	Supply Current (DDR-only mode)	Loaded outputs, 133 MHz			500	mA
I_{DDS}	Supply Current	PWR_DWN# = 0			100	µA
V_{OUT}	Output Voltage Swing	See test circuity (refer to *Figure 1*)	0.7		V_{DD} +0.6	V
V_{OC}	Output Crossing Voltage		(V_{DD}/2) – 0.1	V_{DD}/2	(V_{DD}/2) + 0.1	V
IN_{DC}	Input Clock Duty Cycle		48		52	%

Switching Characteristics [4]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
–	Operating Frequency		66		200	MHz
–	Duty Cycle[3, 5] = $t_2 \div t_1$	Measured at 1.4V for 3.3V outputs Measured at V_{DD}/2 for 2.5V outputs	IN_{DC} – 5%		IN_{DC} + 5%	%
t_3	SDRAM Rising Edge Rate[3]	Measured between 0.4V and 2.4V	1.0		2.75	V/ns
t_4	SDRAM Falling Edge Rate[3]	Measured between 2.4V and 0.4V	1.0		2.75	V/ns
t_{3d}	DDR Rising Edge Rate[3]	Measured between 20% to 80% of output (refer to *Figure 1*)	0.5		1.50	V/ns

Notes:

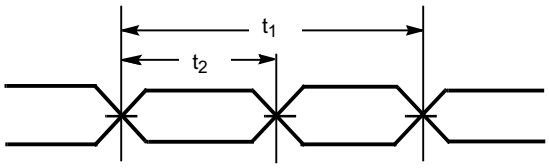
2. **Multiple Supplies**: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Parameter is guaranteed by design and characterization. Not 100% tested in production.
4. All parameters specified with loaded outputs.
5. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1 V/ns.

Switching Characteristics (continued)[4]

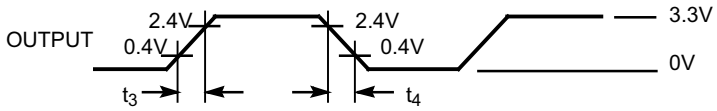
Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t_{4d}	DDR Falling Edge Rate[3]	Measured between 20% to 80% of output (refer to *Figure 1*)	0.5		1.50	V/ns
t_5	Output to Output Skew for DDR[3]	All outputs equally loaded			100	ps
t_6	Output to Output Skew for SDRAM[3]	All outputs equally loaded			150	ps
t_7	SDRAM Buffer LH Prop. Delay[3]	Input edge greater than 1 V/ns	5		10	ns
t_8	SDRAM Buffer HL Prop. Delay[3]	Input edge greater than 1 V/ns	5		10	ns

Switching Waveforms

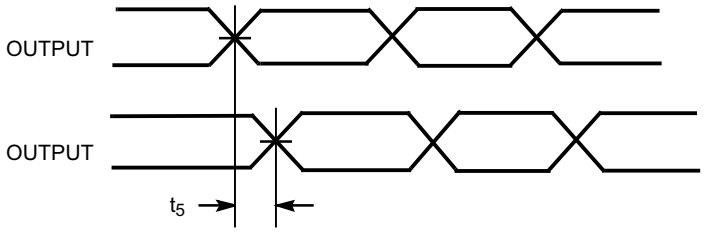
Duty Cycle Timing



All Outputs Rise/Fall Time



Output-Output Skew



SDRAM Buffer HH and LL Propagation Delay

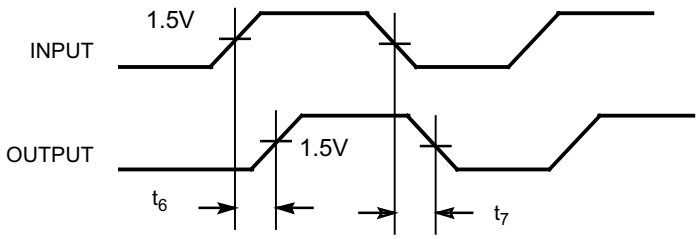


Figure 1 shows the differential clock directly terminated by a 120Ω resistor.

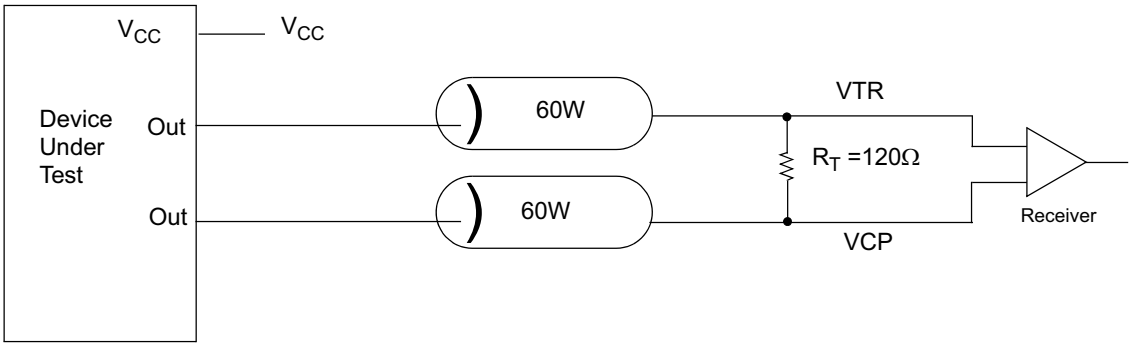
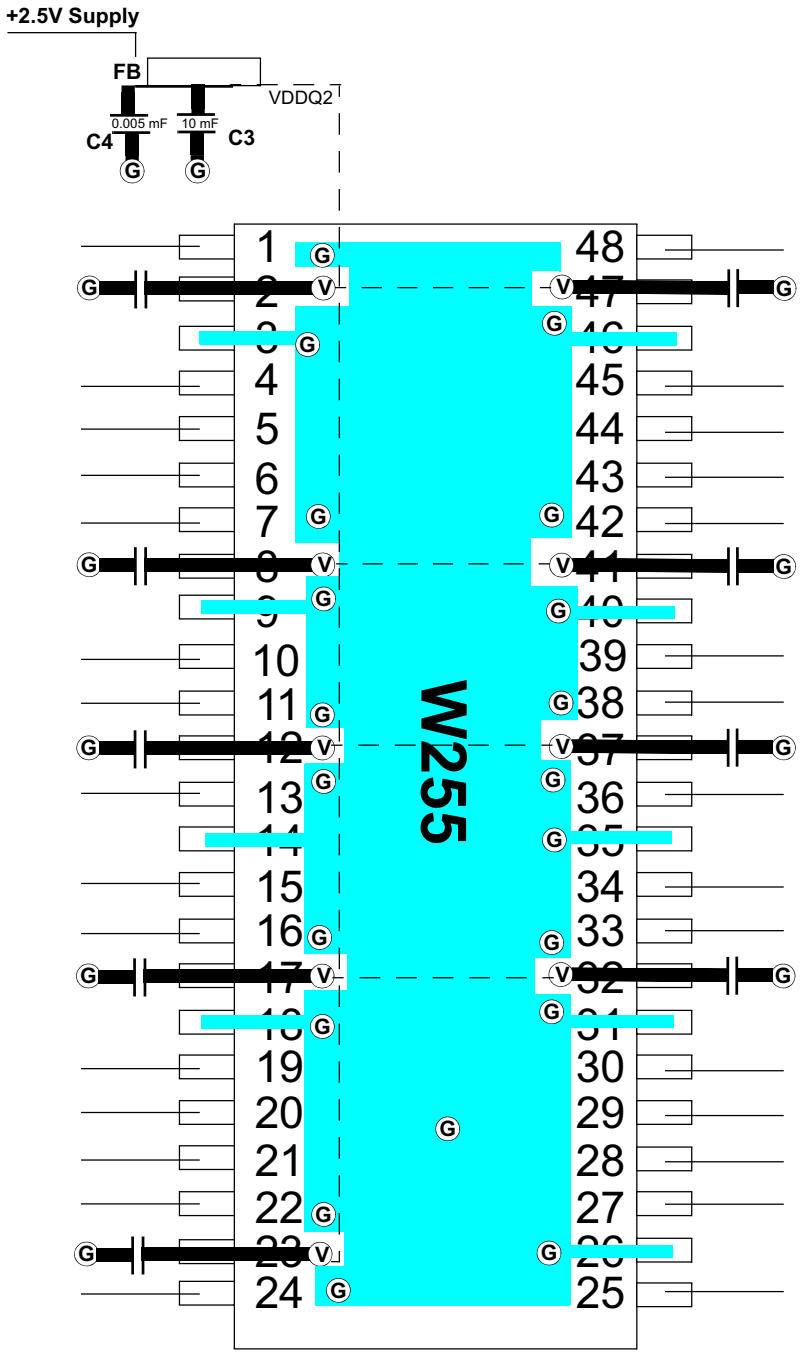


Figure 1. Differential Signal Using Direct Termination Resistor

Layout Example for DDR 2.5V Only



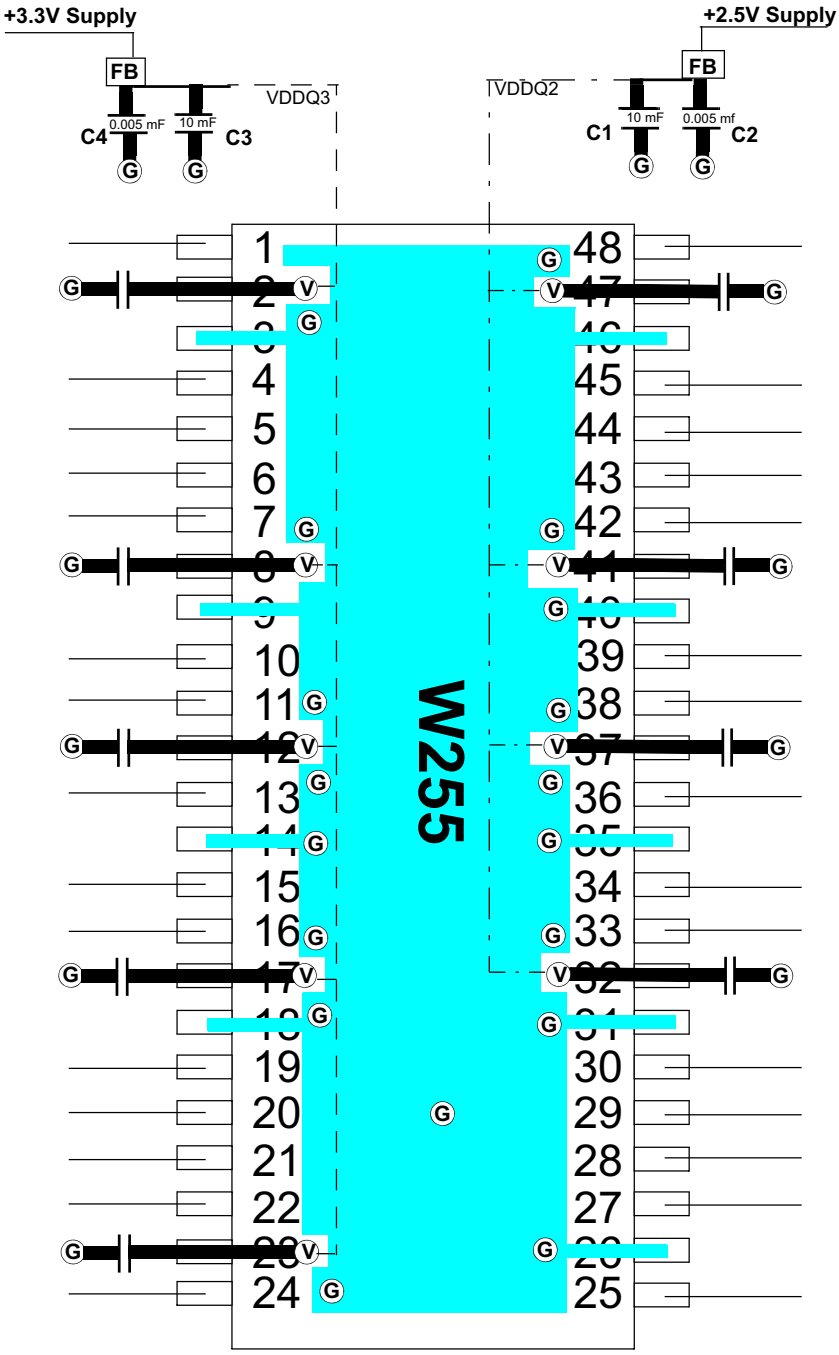
FB = Dale ILB1206 - 300 (300Ω @ 100 MHz) or TDK ACB 2012L-120

Ceramic Caps C3 = 10–22 µF C4 = 0.005 µF

(G) = VIA to GND plane layer (V) = VIA to respective supply plane layer

Note: Each supply plane or strip should have a **ferrite bead and capacitors**
All bypass caps = 0.1 µF ceramic

Layout Example SDRAM (Mixed Voltage)



FB = Dale ILB1206 - 300 (300Ω @ 100 MHz) or TDK ACB 2012L-120

Ceramic Caps C1 and C3 = 10–22 µFC2 & C4 = 0.005 µF C6 = 0.1 µF

Ⓖ = VIA to GND plane layer Ⓥ = VIA to respective supply plane layer

Note: Each supply plane or strip should have a **ferrite bead and capacitors**
All bypass caps = 0.1 µF ceramic

Ordering Information

Ordering Code	Package Type	Operating Range
W255H	48-pin SSOP	Commercial
W255HT	48-pin SSOP–Tape and Reel Option	Commercial
Lead-free		
CYW255OXC	48-pin SSOP	Commercial
CYW255OXCT	48-pin SSOP–Tape and Reel Option	Commercial

Package Drawing and Dimensions

48-lead Shrunk Small Outline Package O48